REMARKS

Claims 1-14, 16-20 and 23-25 are pending. Reconsideration of the Application and Claims is respectfully requested.

Finality of Outstanding Rejection

The outstanding Office Action is identified as being non-final in the Office Action Summary. However, on page 11 of the outstanding Office Action there is included a statement that suggests that the Office Action is Final. Applicant respectfully requests that in the next Office Action the non-final status of the outstanding Office Action be acknowledged.

103 Rejection

Claims 1-14, 16-20 and 23-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (US Patent Application No. 2003/0158995) in view of Chan et al. (US Patent No. 6,230,249). Applicant respectfully submits that Lee et al. in view of Chan et al. does not anticipate or render obvious the embodiments of the present invention as are set forth in Claims 1-14, 16-20 and 23-25.

The Examiner is respectfully directed to Claim 1, which is drawn to a variable width memory system. Claim 1 is reproduced below in its entirety for the Examiner's convenient reference.

1. A variable width memory system comprising:
a bus for communicating information;
a plurality of single cell variable width memory locations coupled to said bus, said plurality of single cell variable width memory locations store information, wherein said plurality of single cell variable width memory locations receive a number of bits corresponding to the width of the single cell variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system, wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said

variable width register; and

a controller coupled to said bus, said controller directs access to said plurality of single cell variable width memory locations, wherein said number of bits potentially vary automatically on a per access basis depending on which single cell variable width memory location of said plurality of single cell variable width memory locations is being accessed, wherein all memory locations are not required to have the same width.

Claims 8, 20 and 23 recite limitations that are similar to those recited in Claim 1. Claims 2-7 depend from independent Claim 1, Claims 9-14 and 16-19 depend from independent Claim 8 and Claims 24-25 depend from independent Claim 23 and recite additional limitations of embodiments of the present claimed invention.

Lee et al. does not anticipate or render obvious the embodiments of the present invention that are set forth in Applicant's Claims. Lee et al. is deficient as Lee et al. does not teach or suggest all of the limitations that are recited in the Claims as is required to anticipate or render obvious the embodiments of the present claimed invention set forth therein. In particular, Lee et al. does not teach or suggest a variable width memory system that includes "a plurality of single cell variable width memory locations" that "store information" and that "receive a number of bits corresponding to the width of the variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system" wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations).

Claims 1, 8, 20 and 23 have each been amended to include the aforementioned limitation drawn to the relationship between the recited single cell variable width memory locations and the recited variable width register. Support for the newly added limitation can be found in Applicant's specification at page 10, lines 10-23. It is important to note that the

newly added limitation specifically delimits the type of process that is involved in relating the recited single cell variable width memory locations and the recited variable width register. This limitation (along with the others recited in the Claims) must be taught or suggested by the cited reference in order for a proper prima facie case for rejection to be supported thereby. However, Applicant respectfully submits that the newly added limitation is not taught or suggested anywhere by the cited references. If a rejection based on the cited references is maintained Applicant respectfully requests that the location in the references where the aforementioned limitation is taught or suggested be identified.

Lee et al. only discloses a dissimilar method for DRAM control with adjustable page size. Lee discloses that as a part of the disclosed method for DRAM control, page size can be adjusted by using memory masks. It should be noted that Lee et al. is concerned with adjusting page size and is not concerned with adjusting the width of a single cell memory location (e.g., a cell) as is required to meet the limitations of Applicant's Claim 1 (Claims 8, 20 and 23 contain similar limitations). However, assuming arguendo that such is shown, Lee et al. certainly does not associate a width of a variable width register, that is located in a processor associated with the variable width memory system, with the width of a single cell variable width memory location as is required to meet the limitations of Claim 1 (Claims 8, 20 and 23 contain similar limitations). Furthermore, there is nothing in Lee et al. that suggests that bits are received that correspond both to the width of a variable width memory location and to the width of a variable width register that is located in a processor. It is important to note that in order to meet the aforementioned limitations of Claim 1 a reference must teach that both the variable width memory locations and the variable width registers correspond to the bits that are received.

Based upon Applicants review of the Lee et al. reference, Applicants respectfully submit that nowhere therein is a variable width memory system that includes a plurality of single cell variable width memory locations that store information and that receive a number of bits corresponding to the width of the variable width memory locations and the width of a register that is located in the processor that is associated with the variable width memory taught or suggested as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations). Moreover, nowhere therein is the newly added Claim limitation "wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register" taught or suggested.

Chan et al. does not teach or suggest a modification of Lee et al. that would remedy the deficiencies of Lee et al. outlined above. In particular, Chan et al. does not teach or suggest a variable width memory system that includes "a plurality of single cell variable width memory locations" that "store information" and that "receive a number of bits corresponding to the width of the variable width memory locations and the width of a variable width register that is located in a processor associated with the variable width memory system" wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register as is set forth in Claim 1 (Claims 8, 20 and 23 contain similar limitations). Chan et al. only discloses a dissimilar method and apparatus for providing logical cell available information in a memory. However, nowhere in the Chan et al. reference is the number of bits that are received into a memory location associated with the width of a variable width memory location and a variable width register that is located in a processor associated with the variable width memory system or any register for that matter. Moreover, nowhere therein is the newly added Claim limitation

"wherein a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register" taught or suggested.

The Examiner contends on page 4 of the outstanding Office Action (bottom of the page) that simply because Chan et al. contains a counter and a comparator that store "values for their functions," this somehow teaches or suggests that the Chan et al. system includes a processor that contains variable width registers that read on the above discussed limitation of Claim 1 (Claims 8, 20 and 23 recite similar limitations). Applicants respectfully disagree with this logic. Assuming arguendo that there is a processor associated with the Chan et al. system there is absolutely nothing that necessitates that the registers have variable widths and that the variable widths of these registers be controlled by bits received by the system. Thus assuming arguendo that the Chan et al. system includes a processor that includes registers, there would still exist significant and multifaceted differences between what is currently claimed and what is disclosed by the combination of Lee et al. and Chan et al.

Applicant's dependent Claims provide additional novel subject matter. For example as it regards Claim 4, Applicant respectfully submits that nowhere in the Lee et al. and Chan et al. references is a variable width memory system disclosed as set forth in Claim 1 wherein each one of a plurality of "single cell variable width memory locations is identified by a unique internal identifier which is referenced by said controller to access said each one of said plurality of single cell variable width memory locations" as recited in Claim 4.

As it regards Claim 5, Applicant respectfully submits that nowhere in the Lee et al. and Chan et al. references is a variable width memory system disclosed as set forth in Claim 1 "wherein each one of said plurality of single cell variable width memory locations is

identified by a unique internal identifier which is referenced by said controller to access said each one of said plurality of single cell variable width memory locations" as recited in Claim 5.

As it regards Claim 7, Applicant respectfully submits that nowhere in the Lee et al. and Chan et al. references is a variable width memory system disclosed as set forth in Claim 1 "wherein the bit width of at least one of said plurality of single cell variable width memory locations is configured in accordance with criteria directed at decreasing processor operations" as recited in Claim 7.

Consequently, the embodiments of present invention that are set forth in Claims 1, 8, 20 and 23 are not anticipated or rendered obvious by Lee et al. in view of Chan et al. Accordingly, Applicant respectfully submits that Lee et al. in view of Chan et al. does not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 2-7 which depend from Claim 1, Claims 9-14 and 16-19 which depend from Claim 8, and Claims 24-25 which depend from Claim 23. Consequently, the rejection of Claims 1-14, 16-20 and 23-25 under 35 U.S.C. 103(a) is improper and should be withdrawn.

Conclusion

In light of the above-listed amendments and remarks, Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact Applicant's representative Bill O'Meara whose telephone number is (970) 898-7917 if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 10/19, 2007

James P. Hao
Registration No. 36,398
Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060